An Integrated Solution for Basics Digital Electronics: Boole-DEUSTO and WebLab-DEUSTO

J. García-Zubía[1], L. Rodríguez-Gil[1], P. Orduña[2], I. Angulo[1], U. Hernandez-Jayo[1], O. Dziabenko[2], ML. Güenaga[2], R. Artiach[3]

[1] Faculty of Engineering - University of Deusto, Bilbao, Spain
[2] DeustoTech Learning – University of Deusto, Bilbao, Spain
[3] Urdaneta School, Bilbao, Spain

***Abstract*—The software BOOLE-DEUSTO is oriented to the design of digital electronic circuits from the student point of view. On the other hand, WebLab-DEUSTO is a well known remote laboratory, and one of the implemented experiments is focused on CPLD and digital electronics. The objective of this paper is to describe the results of connecting BOOLE-DEUSTO and WebLab-DEUSTO. Under this common approach, a novel student can design a digital circuit using K maps, truth tables, Boolean expressions, etc. and then, automatically, he/she can implement, download and see the real circuit in the remote lab.**

***Index Terms* — remote experiments, digital electronics.**

I. INTRODUCTION

From a methodological point of view, to design a digital circuit at the bit-level consists on transforming every representation into the next one. In a bit-level combinational digital circuit, the different representations are: text, truth table, V-K maps, Boolean expressions and digital circuits using AND, OR and NOT logic gates (or NAND/NOR gates). In a bit-level sequential digital circuit (Finite State Machine), the different representations are: text, FSM diagram (Moore or Mealy), truth table, Boolean expressions and digital circuit using J-K or D flip-flops.

This process is followed step by step by teachers/students. The next step in this process is the implementation of the digital circuit. To do this the teacher/students can follow two main directions: 74XX integrated circuits and programmable devices (microcontrollers, CPLD, FPGA, etc.). It is very popular to use CPLD/FPGA devices to implement digital circuits. Under this approach, the student must obtain a new representation of the system using the VHDL programming language in a complex design environment (ISE Xilinx, etc.).

This paper shows how to connect these representations; truth table, V-K diagrams, digital circuit… (what is more related with the students and the classroom) with the real devices (CPLD/FPGA) in the laboratory. This process is implemented connecting BOOLE-DEUSTO (a software tool for digital circuits design) and WebLab-DEUSTO (remote laboratory).

II. BOOLE-DEUSTO SW FOR DIGITAL ELECTRONICS

The software BOOLE-DEUSTO [1] is a Boolean calculator for the students and its first version was designed in 2000. They are able to design step by step a digital circuit using the same method as the one used in the classroom.

In general, the design process of a digital circuit at bit level is made up of different steps. After reading the statement, the teacher/student will obtain the truth table, the V-K map, the minimized Boolean expression and the digital circuit using AND-OR, NAND or NOR gates.

In Boole-Deusto, the user writes a name for the system and shows the number of inputs and outputs. After doing this, Boole-Deusto offers the user different ways to describe the system (Fig. 1): truth table, V-K maps, etc.

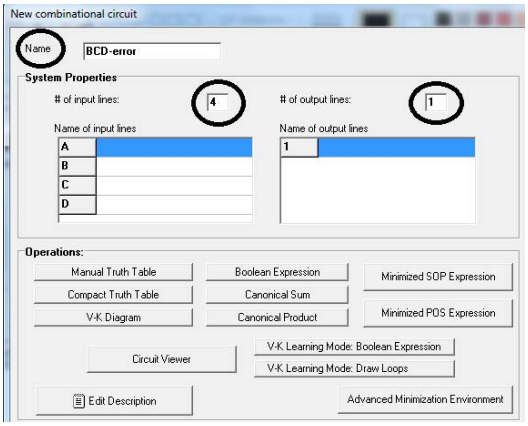


Figure 1. Description of a combinational digital circuit

Fig. 2 shows the truth table of a BCD error detector. It shows that the combinations 1010–1111 activate the output.

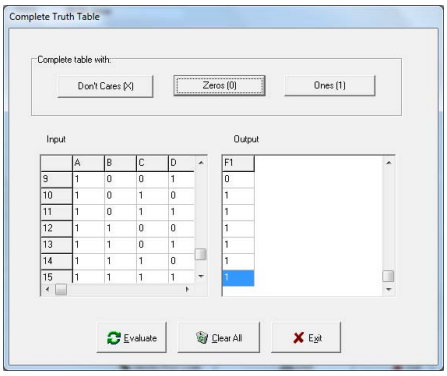


Figure 2. Truth table of the BCD error detector

At this moment the student can see the V-K map or even he or she can modify it. And after this, Boole-Deusto can show the solved V-K map with the loops and the Boolean expressions (Fig. 3).

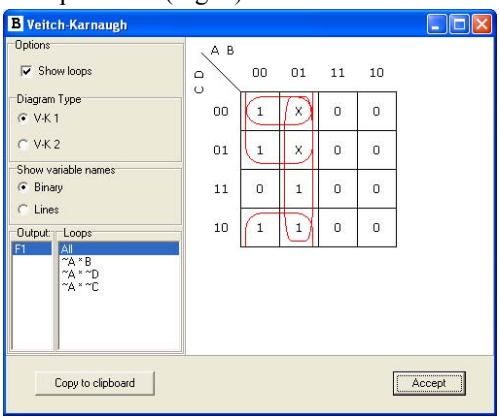


Figure 3. The solved V-K map of the BCD error detector

Finally, the student can see the digital circuit implemented with AND-OR , NAND or NOR logic gates. The circuits shown in Fig. 4 can not be simulated, they are only images.

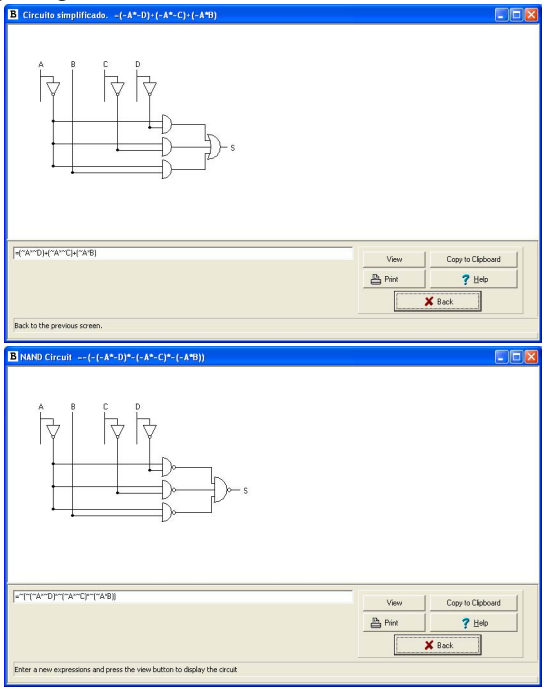


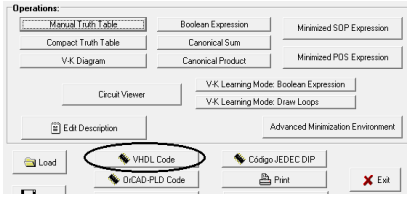
Figure 4. AND-OR and NAND digital circuits

The main difference between BOOLE-DEUSTO and other professional software tools (Proteus, OrCAD, etc.) is that BOOLE-DEUSTO is educational software and oriented to learning outcomes, while Proteus is focused to industrial companies to obtain real circuits [2]. But the two points of view are needed:

- Boole-Deusto is more centered in the process of obtaining of the digital circuit, for example V-K maps.
- Proteus is more centered in the results than in the process.

After this process, if the student wants to see the digital circuit in real operation, he or she has two options (at least two options): to make the circuit with cables and integrated circuits or to use a programmable device like CPLD/FPGA or a microcontroller.

BOOLE-DEUSTO offers the users the possibility of obtaining a VHDL file with the description of the system. Fig. 5 shows the VHDL description of the BCD error detector.




```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity BCD-error is
      Port (
            A: in std_logic;
            B: in std_logic;
            C: in std_logic;
            D: in std_logic;
            S0: out std_logic
            );
end BCD-error;

architecture behavioral of BCD-error is
begin
      S0<=((A and C) or (A and B));
end behavioral;
```

Figure 5. VHDL file with the system description.

Additionally the user must assign to each input and output one pin of the FPGA or CPLD board in a file. To obtain the UCF file (user constrains file), the user needs to know where the pins are. Table 1 shows the pins assigned to six switches and leds.

TABLE I. RELATION BETWEEN INPUTS/OUTPUTS AND PINS OF THE CPLD&FPGA BOARDS

Inputs	FPGA pin	CPLD pin	Outputs	FPGA pin	CPLD pin
switch 5	E15	P66	led 5	N12	P6
switch 4	E16	P67	led 4	P13	P5
switch 3	F15	P68	led 3	N14	P4
switch 2	G15	P69	led 2	L12	P3
switch 1	G16	P71	led 1	P14	P2
switch 0	H15	P70	led 0	K12	P1

The UCF with the assignation for the BCD error detector is in Fig. 6. It is a very simple txt file.

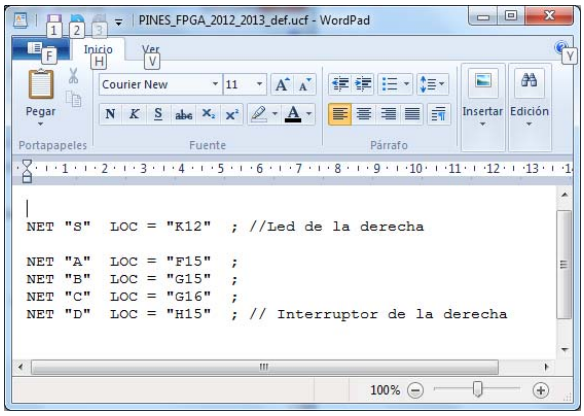


Figure 6. UCF for the BCD error detector

This software tool can be used for combinational (logic gates) and for sequential (Finite State Machines) digital circuits.

Fig. 7 shows the use of the Boole-DEUSTO to implement a Moore FSM that detects in the input sequence three or more 1s.

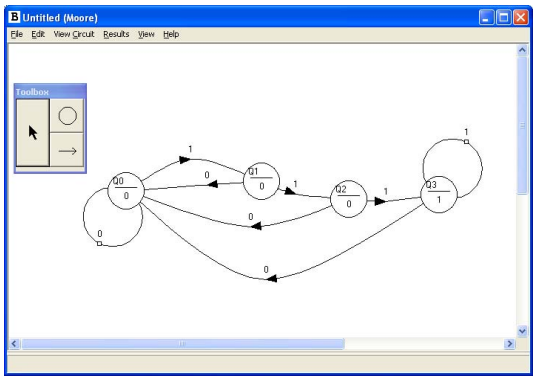


Figure 7. FSM of the sequence detector "111".

Again, the student can obtain the digital circuit and the VHDL description, as it is shown in Fig. 8.

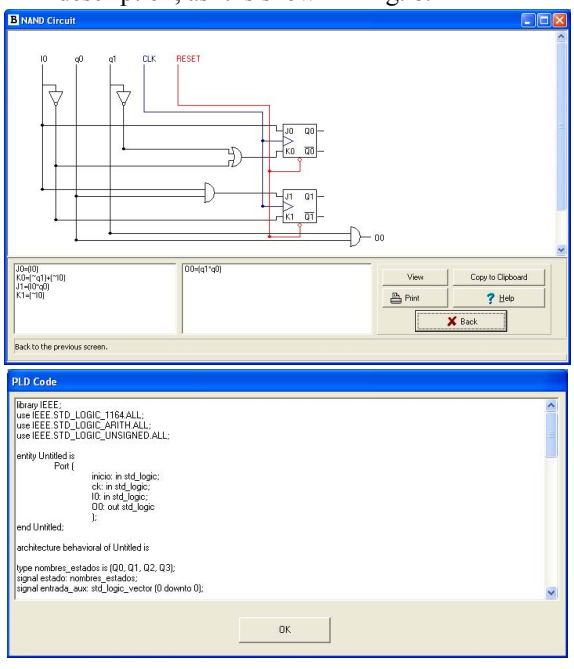


Figure 8. FSM's descriptions: digital circuit and VHDL program

The VHDL program can be implemented using a FPGA or CPLD device and a software environment. In the University of Deusto we use Xilinx devices and the ISE WebPack Free environment [3].

III. WEBLAB-DEUSTO REMOTE LAB

At this moment, the Faculty of Engineering of the University of Deusto offers students a classical laboratory for digital electronics based in Digilent FPGA educational boards and it also offers the WebLab-Deusto. The two options are freely managed by the student. He or she can design and implement his or her systems using a real board or the remote lab. Even the students can buy these educational boards because they are cheap (around $ 50 for a CPLD board and $ 150 for a FPGA board). Digilent is the best well known company [4] in CPLD&FPGA educational boards. From our point of view there is not a competition among the different options, we do not have to decide which is the best option, simply we offer all of them to the students. They will decide depending on their needs, and this election can change week by week. It is up the students.

To sum up, the major advantage of a remote lab is that it can be used everywhere and at any time by the student, and he or she only needs an Internet connection. On the other hand, with a real board, the student improves the sense of reality and can interact with other students.

WebLab-Deusto [5] is a remote lab that allows users to make real experiments using the Internet connection. It includes different devices and experiments: PIC microcontroller, microbot, a toy submarine, Xilinx CPLD, Xilinx FPGA, VISIR LXI and an experiment with logic gates. Fig. 9 shows the WebLab-Deusto Web page with the different offered experiments.

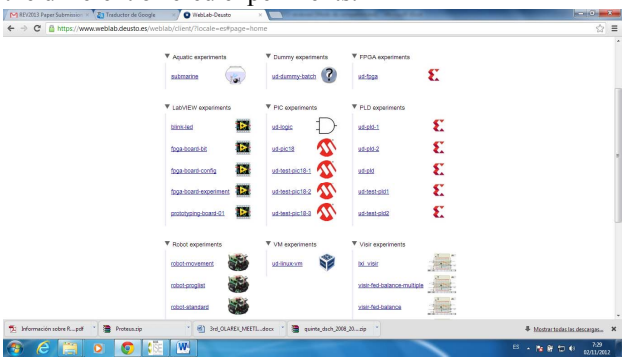


Figure 9. WebLab-Deusto web page with the experiments available

WebLab-Deusto is an Open Source (GNU GPL) [6] platform for remote experimentation. The remote experiments offered by Weblab-Deusto can be accessed using any Web browser and any operating system through a PC, laptop, tablet, smart phone, etc. WebLab-Deusto offers administration tools like access control, login, etc. and supports federation and load balance of remote experiments. It is being used since 2004.

There are more platforms for remote experimentation like iLAB or labShare [7] and there are also others implementations of FPGA/CPLD remote labs [8, 9].

Attending the CPLD and FPGA devices and the VHDL programs, the remote lab WebLab-DEUSTO allows users to upload a file (.bit for FPGA and .jed for CPLD) to control inputs, and to see the outputs through a webcam.

Fig. 10 shows the Weblab-DEUSTO interface for a CPLD [10].

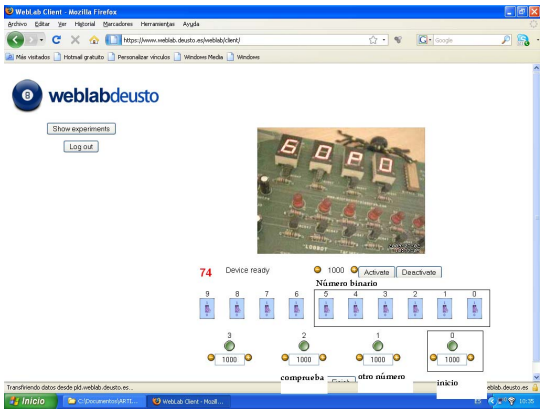


Figure 10. WebLab-DEUSTO remote experiment with a CPLD

Continuing with the process started in Section II, after the obtaining of the VHDL code, the last step is to connect the VHDL file obtained by the student in the BOOLE-DEUSTO environment with the remote experiment implemented by the WebLab-DEUSTO. This process is controlled more or less automatically (see Fig. 11):

- If the student has experience with ISE WebPack (Xilinx), he or she can follow the process by his own: open a new project, add the VHDL source given by Boole-Deusto, integrate it with the UCF file and synthetize-implement the project to obtain the BIT file that will be uploaded in the WebLab-Deusto-FPGA (or the JEDEC file for the WebLab-Deusto-CPLD). But surely in this situation the student will prefer to design his project without the Boole-Deusto, programming it directly in VHDL.
- On the other hand, the novel student will write the truth table or will draw the FSM in Boole-Deusto and the proposed automatic process will create in ISE WebPack the project, will add the UCF file and finally will obtain the BIT file. In this case the student is involved in the description (the behavior), but not in the implementation.

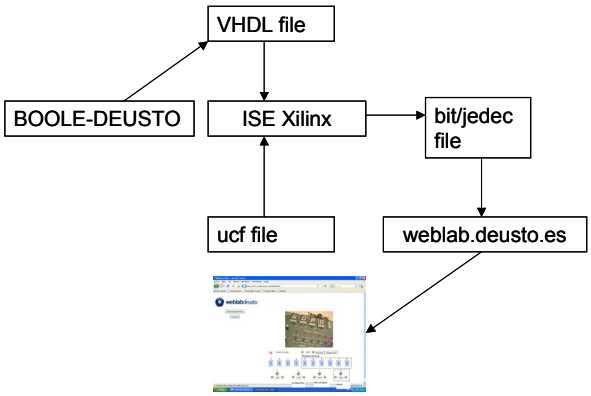


Figure 11. Integration of BOOLE-DEUSTO and WebLab-DEUSTO

In the second scenario, the ISE environment will be in the server side, so in this case the student will upload the VHDL code (generated by the Boole-Deusto) and the UCF file, and the proposed system will obtain automatically the BIT file, and after this the FPGA will be programmed. After two minutes, the student will see the interface of Fig. 9 and he or she will control the inputs (10 switches and 4 buttons) and will see the outputs through the webcam (six leds and one 7-segments). At present, there is a prototype of this automated process, but the final version is still under design.

With the combination of Boole-Deusto and WebLab-Deusto, the user can follow step by step the design and implementation of a digital circuit.

From the teacher point of view, he or she can design and implement in the classroom a digital circuit in front of the students. During this process –using a video projector- all the students will see at the same time the system running, so the teacher can analyze the system through a real experiment, not with a simulation or something similar. This strategy can be a powerful tool for teachers, not only in the university, but also in the schools.

IV. OLAREX PROJECT

The combination of Boole-DEUSTO and WebLab-DEUSTO is being developed in the OLAREX project funded by the EU to enhance and modernize STEM curricula, foster student´s creativity and motivation, and develop professional e-didactic and technology competences and skills (see Fig. 12).

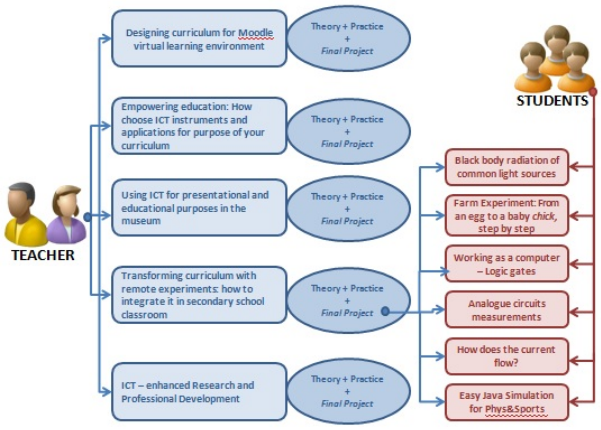


Figure 12. OLAREX Project: learning modules

One part of the project is to train participants, and after this they will:

(1) improve e-didactic competences;
(2) know the basic theory of remote experiments, how to access a remote laboratory;
(3) be able to create new e-learning materials, courses, and remote experiments.

One module is related with digital electronics and it is being implemented with Boole-DEUSTO and WebLab-DEUSTO. This module will be used in the subject "Technology" in the last semester of the secondary school with students 16 - 17 years old. It will be used in Urdaneta School (Bizkaia, Spain).

The main objective of this part of the subject is to learn about the basis of digital electronics: Boolean algebra, logic gates, integrated circuits, etc. The system proposed will allow the teacher and the students to implement real digital circuits to reinforce the theoretical concepts introduced.

In general it is very difficult for secondary schools to create and maintain laboratories in the field of digital electronics (it is not their main focus), but with the system proposed students and teachers can implement real systems without economic and technological efforts, they should only be concentrated in the description of the digital circuit, not in the technical side.

At this moment this module is under development together with URDANETA School in Bilbao (Spain), and after its use in the classroom the results will be analyzed.

V. Conclusions and Future Work

The integration of BOOLE-DEUSTO and WebLab-DEUSTO allows the student to design and test a real digital circuit in an easy way.

Under this approach, the student not only can improve his autonomous work, but also he or she can work in a real scenario (the remote lab is a real laboratory connected through Internet) without being observed by the teacher.

This combination can be used by teachers to teach, and by students to learn in autonomous way.

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Authors

J. Garcia Zubia, is with the University of Deusto, Faculty of Engineering, Avda de las Universidades 24, 48007 Bilbao, Spain (e-mail: zubia@deusto.es).

L. Rodríguez-Gil, is with the University of Deusto, Faculty of Engineering, Avda de las Universidades 24, 48007 Bilbao, Spain (e-mail: luis.rodriguez@opendeusto.es).

P. Orduna is with the University of Deusto, Deusto Tech Internet, Avda de las Universidades 24, 48007 Bilbao, Spain (e-mail: pablo.orduna@deusto.es).

I. Angulo is with the University of Deusto, Deusto Tech Mobility, Avda de las Universidades 24, 48007 Bilbao, Spain (e-mail: ignacio.angulo@deusto.es).

U. Hernández-Jayo is with the University of Deusto, Faculty of Engineering, Avda de las Universidades 24, 48007 Bilbao, Spain (e-mail: unai.hernandez@ deusto.es).

O. Dziabenko is with the University of Deusto, Deusto Tech Learning, Avda de las Universidades 24, 48007 Bilbao, Spain (e-mail: olga.dziabenko@ deusto.es).

ML. Güenaga is with the University of Deusto, Deusto Tech Learning, Avda de las Universidades 24, 48007 Bilbao, Spain (e-mail: mlguenaga@ deusto.es).

R. Artiach is with the Urdaneta School, Lauroeta Etorbidea, 6 48180 Loiu, Spain las Universidades 24, 48007 Bilbao, Spain (e-mail: amon.artiach@colegiourdaneta.com).

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