Integration of a Remote Lab in a Software Tool for Digital Electronics

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***Abstract*—The combination of Boole-Deusto (software tool for digital electronics design) and WebLab-Deusto-FPGA (remote lab) allows teachers and students to complete the full design cycle in a computer in only a few minutes: from the truth table or FSM to the real implementation in a FPGA. The system described is oriented towards a first year course in digital electronics to help students and teachers when they are learning and teaching digital electronics.**

Keywords—remote laboratories, digital electronics

I. Introduction

It is very common in the field of digital electronics to teach using software tools for the analysis and design stage, and then laboratories to implement the designed circuits. But from the point of view of teachers and students, not all approaches are equally effective.

This demo paper presents the Boole-Deusto software tool. This tool takes students through the design process first (truth table, K maps, etc.) and then also through the implementation process, using a remote laboratory: WebLab-Deusto-FPGA. Boole-Deusto-FPGA allows users (teachers or students) to go through the whole process, from the description to the physical implementation and testing, in just a few minutes.

Boole-Deusto-FPGA is part of the OLAREX project to promote and to facilitate science and technology among young people in secondary schools.

II. Boole-Deusto

The Boole-Deusto software tool was developed and released for the first time around 2000 [1]. Its main objective was to help teachers and students in the teaching and learning process of digital electronics, especially for introductory courses (first year).

Digital electronics can be divided in two types. Bit-level digital systems, which are based on logic gates (AND, OR, NOT) and flip-flops (D, J-K), and word-level digital systems, which are based on integrated circuits (adders, encoders, multiplexers, counters, etc). Boole-Deusto focuses on bit-level systems.

The creation of a combinational digital system starts with the problem statement and finishes with the digital circuit that implements its solution. This follows a methodological process. Firstly, the problem statement is translated into a truth table. Secondly, the Karnaugh maps are obtained (from the truth table) to minimize the Boolean equation. Finally, the resulting equation is transformed into either a logic gates based digital circuit or a VHDL program (Fig. 1).

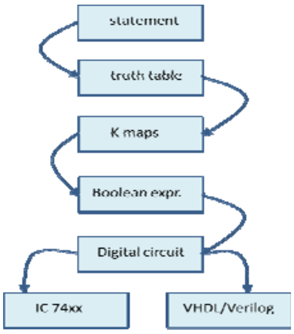
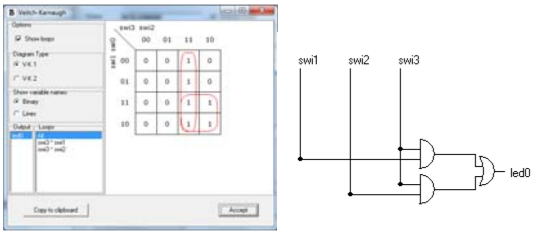


Fig. 1. Design process of a bit-level combinational circuit.

In general, professional software tools like Proteus, LogicSim, etc. do not help the teachers and students in all the steps, because their focus is only in the result: the digital circuit. Through Boole-Deusto, however, users can be taken through all the process step by step, providing them with full control, allowing them to modify the system at any stage.

Fig. 2 describes the process of designing a BCD error detector: if the input (four switches) is not a BCD code, then the output (one led) will be 1.


Veitch-Karnaugh

Options
☑ Show loops

Diagram Type
● V-K 1
○ V-K 2

Show variable names
● Binary
○ Lines

Output: led0
Loops: All
swi3 * swi1
swi3 * swi2

swi1 swi0 \ swi3 swi2	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	0	0	1	1
10	0	0	1	1

Fig. 2. BCD error detector in Boole-Deusto.

The same approach is used with sequential digital systems. In this case the process starts with the Finite State Machine

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(FSM) and finishes with the digital circuit implemented with flip-flops (Fig. 3).

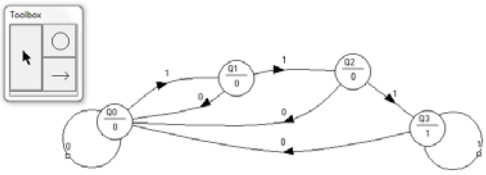


Fig. 3. Sequential digital system in Boole-Deusto.

Currently, Boole-Deusto, which is an Open Source project, has been downloaded thousands of times (see Fig. 4 for downloads since 2007) [2].

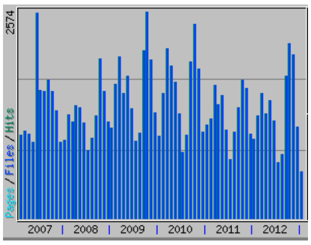
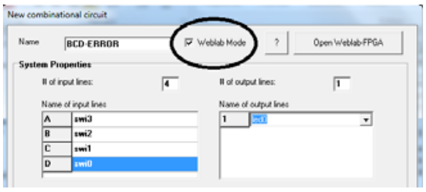


Fig. 4. Statistics of the Boole-Deusto downloads.

After the design process, students can either print a diagram of the circuit or obtain the VHDL program which describes it. Then, they should move to a laboratory to implement that circuit and analyze if it runs properly or not. Generally, as stated, the design is made in a standard classroom or at home, whereas the implementation is made in an electronics laboratory with specialized equipment. The aim of this new approach has been to connect Boole-Deusto with a remote laboratory (WebLab-Deusto), in order for students to be able to remotely test their designs. This is often easy, straightforward and convenient, because no wiring or specialized equipment is required. An internet connection is enough to get the designed system implemented in a real, physical board, and to interact with it and check its response. The Boole-Deusto program does all the work, the students do not wire their circuits nor write VHDL code.

III. Connecting Boole-Deusto to WebLab-Deusto

Once users finish the design process users can click on the WebLab-Deusto button to directly access a FPGA controlled by WebLab-Deusto.


New combinational circuit

Name: BCD-ERROR

☑ Weblab Mode

System Properties

# of input lines: 4

# of output lines: 1

Name of input lines

A	swi3
B	swi2
C	swi1
D	swi0

Name of output lines

1	led0

Fig. 5. WebLab Mode for combinational systems

When this is done, a browser will be opened. Once the VHDL file that Boole-Deusto generates has been uploaded, the code is automatically synthesized and programmed into the remote FPGA board. Once this process has finished, users will not only be able to see how the system runs, but interact with it through virtual switches and buttons, as well. For instance, if we have implemented the BCD error detector that we mentioned previously, and users introduce 1010 with the switches, they will soon see the LED turn on.

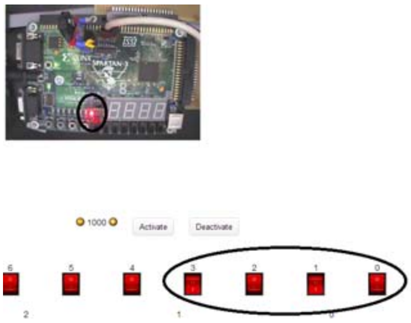


Fig. 6. BCD-ERROR system in WebLab-Deusto, running properly.

The next step involves improving the user experience and increasing the educational potential of the experiments through augmented reality. A virtual model of a system is shown alongside the FPGA board. Then, the FPGA board can be used to control that virtual model, just as if it was being used to control a real appliance, resembling more closely a real-life scenario.

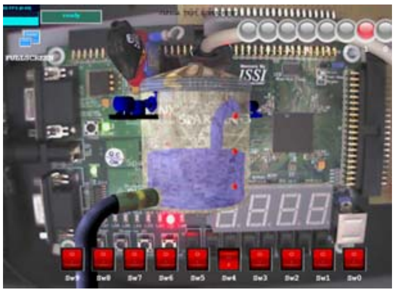


Fig. 7. FPGA watertank experiment running in WebLab-Deusto.

As Fig. 7 shows, the FPGA Watertank experiment displays a virtual water tank over the webcam stream of the board. Watertank control is a potential use of a FPGA. In this case, we have three level-sensors available (represented as small red spheres), two water pumps, and an output (whose flow varies randomly, representing water demand). The aim of the VHDL code to program in the FPGA would be to keep the water level of the deposit between a certain threshold, never overflowing and never going too low.

Technically, the virtual model takes the LEDs as inputs, which lets users control the water pumps easily through VHDL code. The virtual sensor inputs are also readily available to the VHDL code, replacing some of the switches that can normally be controlled manually.

References

[1] Garcia-Zubia, J. “Educational software for digital electronics: Boole-Deusto”, Proc. of IEEE Int. Conf. on MSE, pp: 20 – 22, 2003.

[2] paginaspersonales.deusto.es\zubia